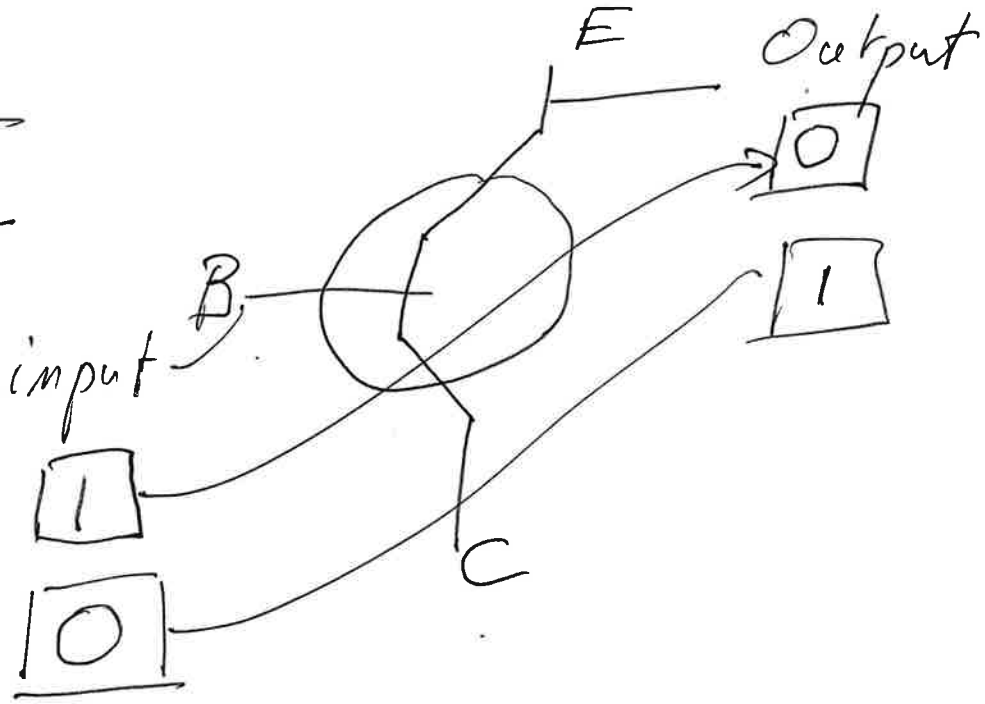
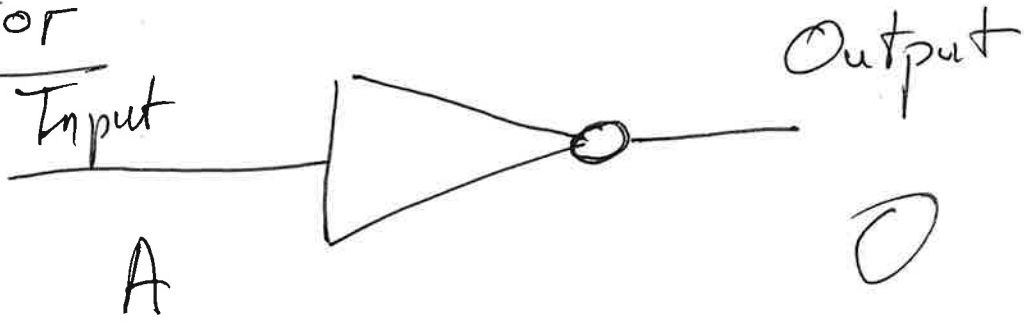
Logic gates 1/26

I. Recap

Transistor

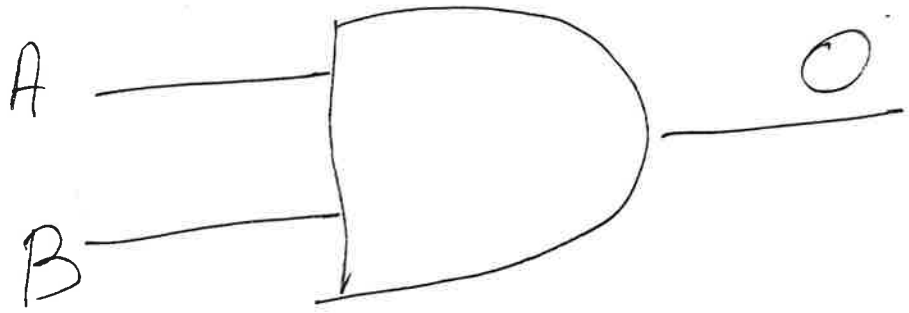


Inverter



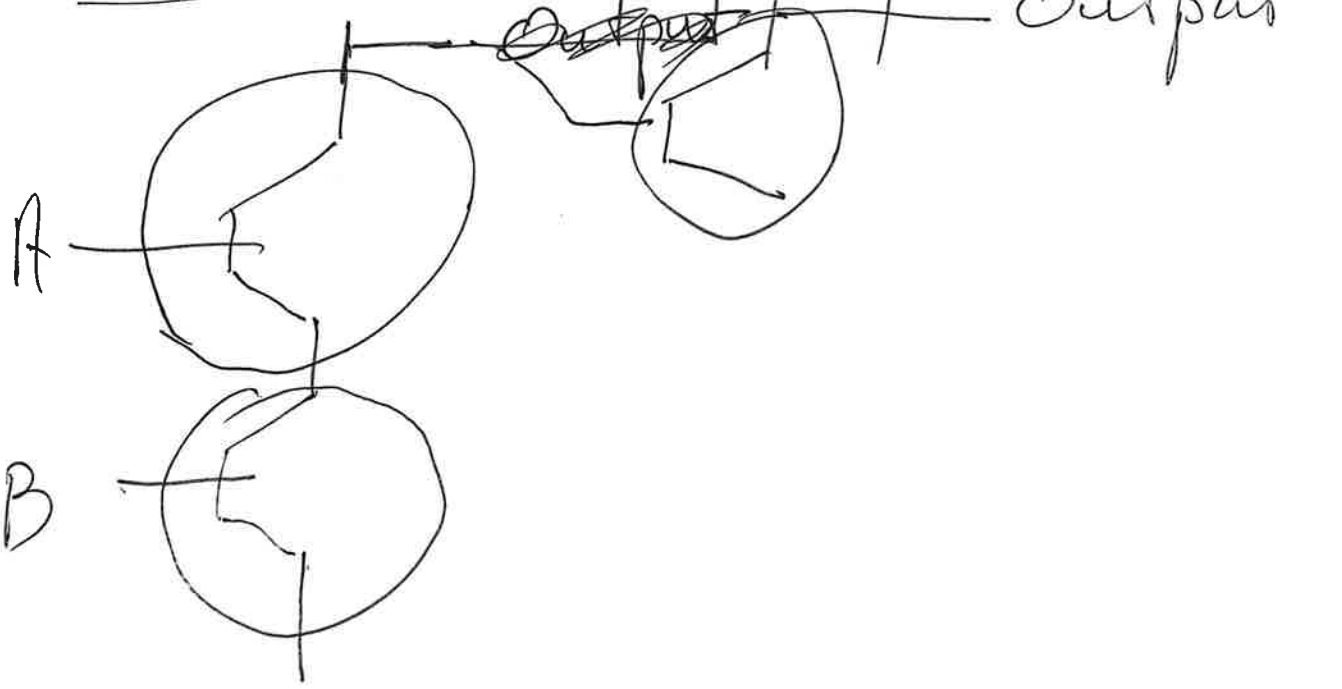
A	O ≡ $\overline{A}$
1	0
0	1

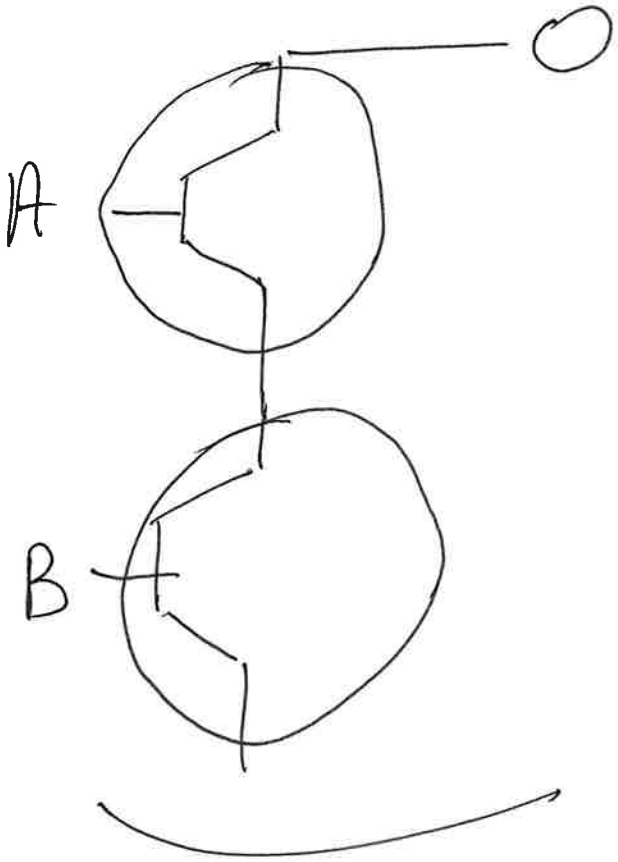
Multiplication : AND gate



A	B	O
1	1	1
1	0	0
0	1	0
0	0	0

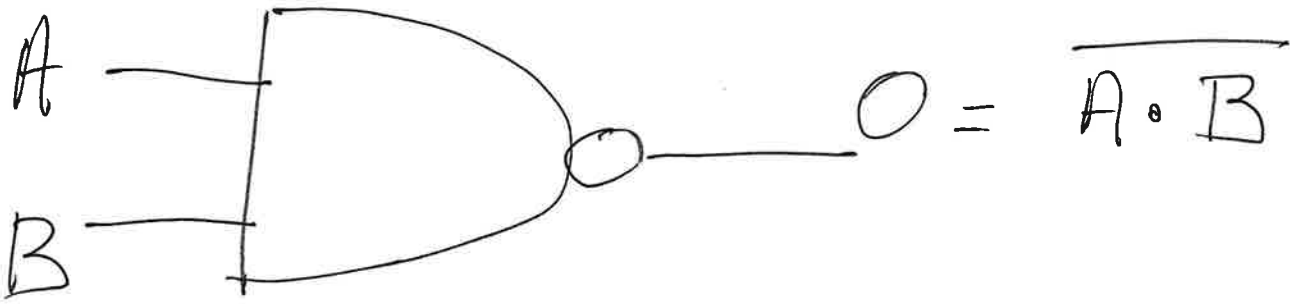
$\equiv A \cdot B$





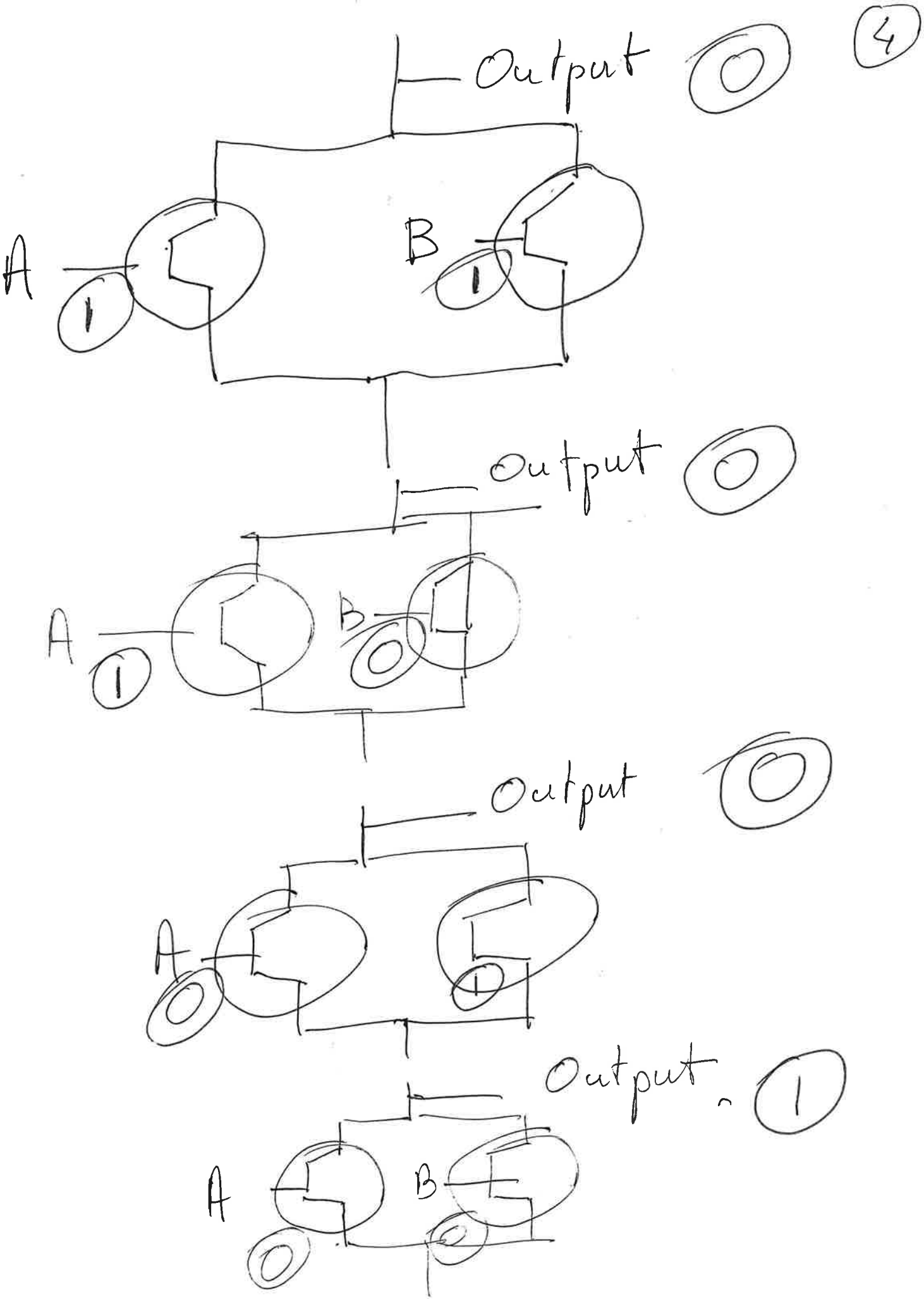
A	B	O
1	1	0
1	0	1
0	1	1
0	0	1

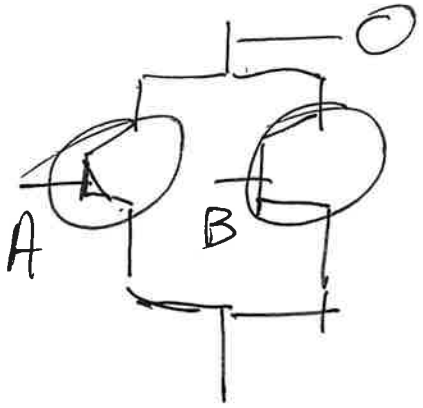
This is refered to as the NAND



II Addition

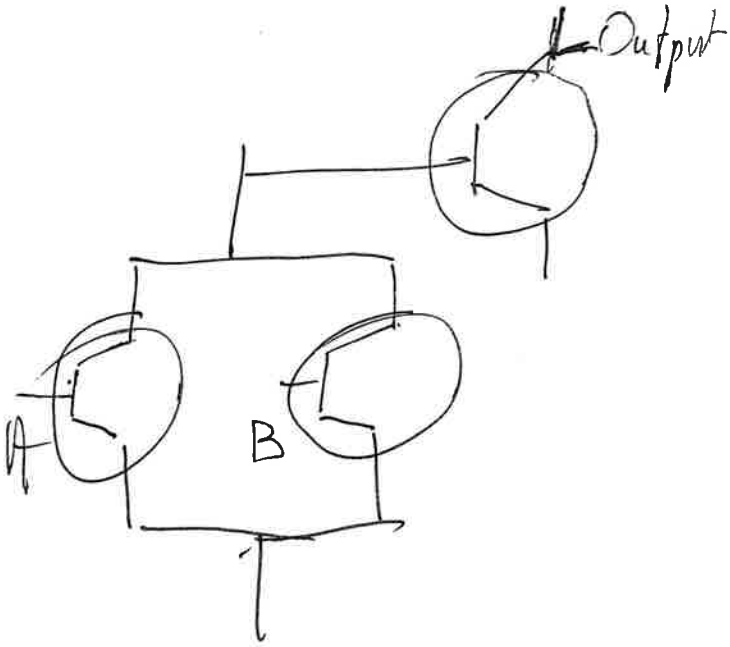
A	B	"A + B"
1	1	1
1	0	1
0	1	1
0	0	0


Output
A
B
1
Output
A
B
1
Output
A
Output
A
B



A	B	O
1	1	0
1	0	0
0	1	0
0	0	1

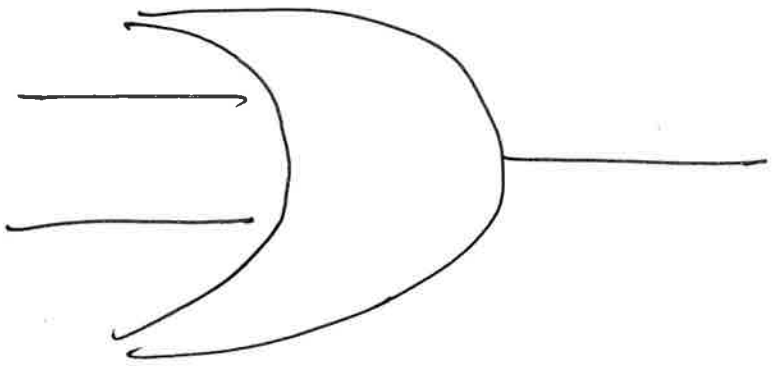
NOR



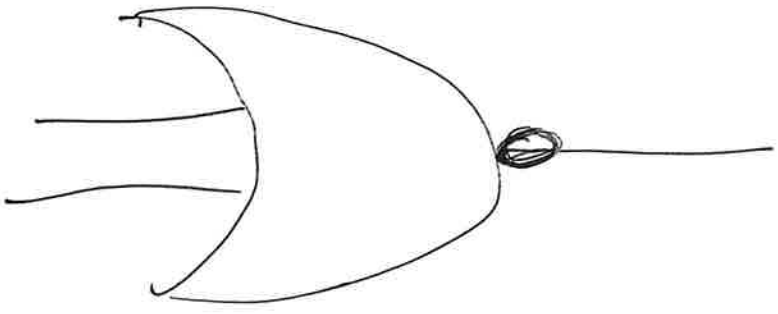
A	B	O
1	1	1
1	0	1
0	1	1
0	0	0

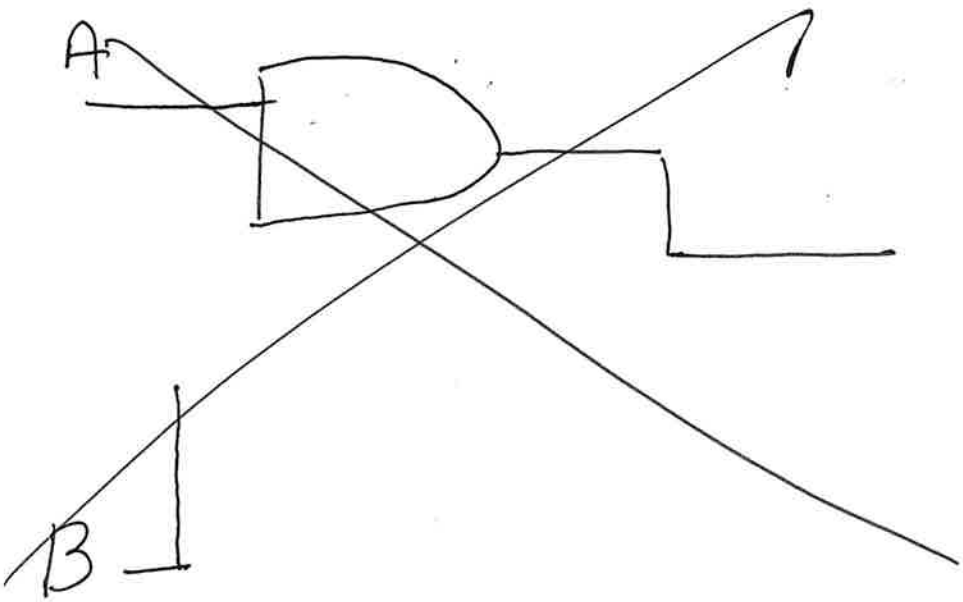
OR

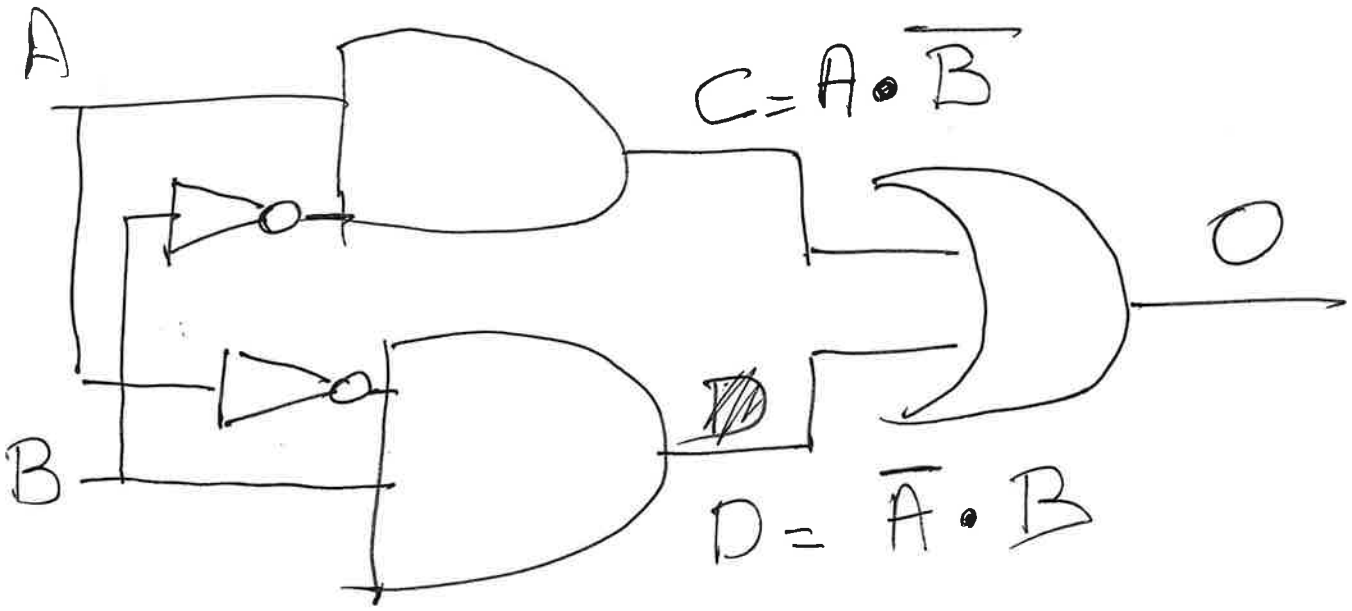
OR gate



NOR gate







A	B	$\overline{B}$	$C = A \cdot \overline{B}$	$\overline{A}$	$D = \overline{A} \cdot B$	O
1	1	0	0	0	0	0
1	0	1	1	0	0	1
0	1	0	0	1	1	1
0	0	1	0	1	0	0

A	B	$A\bar{B} + \bar{A}B$	$OR = A + B$
1	1	0	1
1	0	1	1
0	1	1	1
0	0	0	0

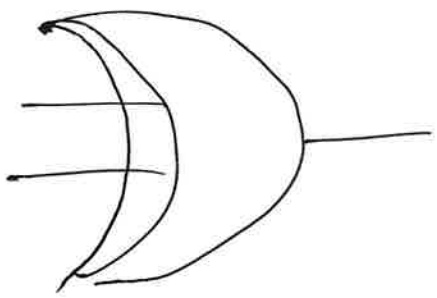
Exclusive OR

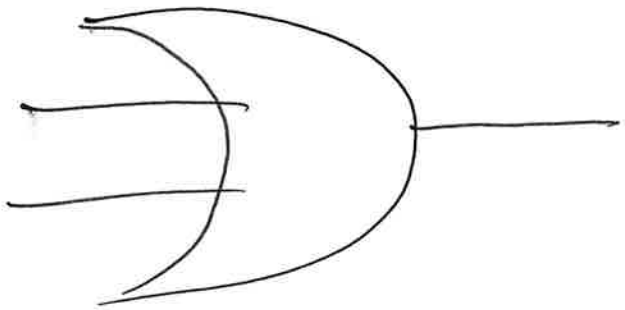
inclusive OR

XOR

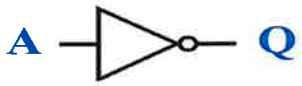
$A \oplus B$

$A + B$





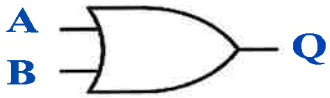
NOT



$\overline{A}$ or $\neg A$

Input	Output
A	Q
1	0
0	1

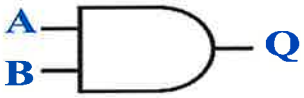
OR



A+B or A∨B

Input 1	Input 2	Output
A	B	Q
1	1	1
1	0	1
0	1	1
0	0	0

AND



A•B or A∧B

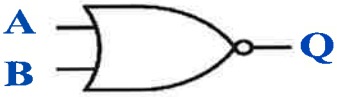
Input 1	Input 2	Output
A	B	Q
1	1	1
1	0	0
0	1	0
0	0	0

XOR

A⊕ B

Input 1	Input 2	Output
A	B	Q
1	1	0
1	0	1
0	1	1
0	0	0

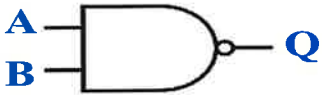
NOR



$\overline{A+B}$ or $\overline{A \vee B}$

Input 1	Input 2	Output
A	B	Q
1	1	0
1	0	0
0	1	0
0	0	1

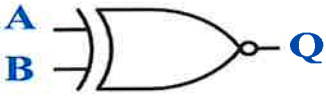
NAND



$\overline{A \cdot B}$ or $\overline{A \wedge B}$

Input 1	Input 2	Output
A	B	Q
1	1	0
1	0	1
0	1	1
0	0	1

XNOR



$\overline{A \oplus B}$

Input 1	Input 2	Output
A	B	Q
1	1	1
1	0	0
0	1	0
0	0	1