Data, Logic, and Computing

ECS 17 (Winter 2026)

Patrice Koehl
koehl@cs.ucdavis.edu

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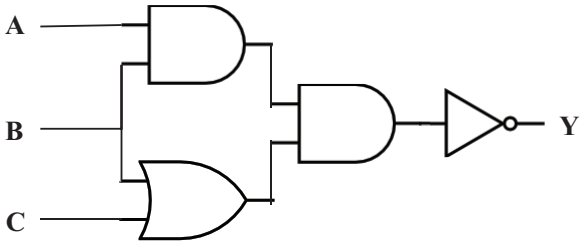
Homework 4

Exercise 1

Find the output/ logic table for this logic gate circuit. Convert it into a Boolean expression



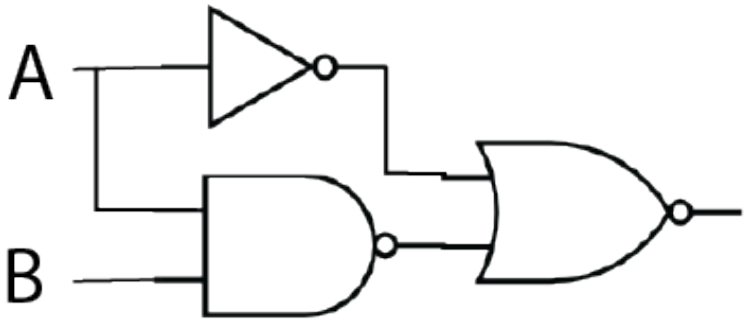
A	B	C	AB	$B+C$	$AB(B+C)$	Y
1	1	1	1	1	1	0
1	1	0	1	1	1	0
1	0	1	0	1	0	1
1	0	0	0	0	0	1
0	1	1	0	1	0	1
0	1	0	0	1	0	1
0	0	1	0	1	0	1
0	0	0	0	0	0	1

The corresponding Boolean expression is $\overline{AB(B+C)}$.

Exercise 2

Find the output/ logic table for this logic gate circuit. Can you find a simpler logic gate that would perform the same operation on A and B?

The corresponding Boolean expression is$\overline{\overline{A}+\overline{AB}}$. Note however that the output of this logic gate is exactly the ouput of the AND logic gate.



A	B	$\overline{A}$	$\overline{AB}$	$\overline{A}+\overline{AB}$	$\overline{\overline{A}+\overline{AB}}$
1	1	0	0	0	1
1	0	0	1	1	0
0	1	1	1	1	0
0	0	1	1	1	0

Exercise 3

Build the logic tables for the Boolean expressions:

a) $\bar{A}B$

A	B	$\bar{A}$	$\bar{A}B$
1	1	0	0
1	0	0	0
0	1	1	1
0	0	1	0

b) $\overline{A\bar{B}}$

A	B	$\bar{B}$	$A\bar{B}$	$\overline{A\bar{B}}$
1	1	0	0	1
1	0	1	1	0
0	1	0	0	1
0	0	1	0	1

c) $A+\bar{B}$

A	B	$\bar{B}$	$A+\bar{B}$
1	1	0	1
1	0	1	1
0	1	0	0
0	0	1	1

d) $\overline{A+\bar{B}}$

A	B	$\bar{B}$	$A+\bar{B}$	$\overline{A+\bar{B}}$
1	1	0	1	0
1	0	1	1	0
0	1	0	0	1
0	0	1	1	0

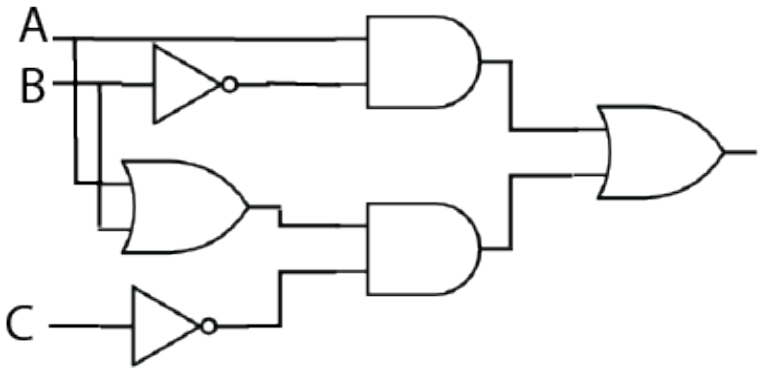
Exercise 3

An engineer hands you a piece of paper with the following Boolean expression on it, and tells you to build a gate circuit to perform that function:

$$A\bar{B} + \bar{C}(A+B)$$

Draw a logic gate circuit for this function. Build its logic table

One solution is:



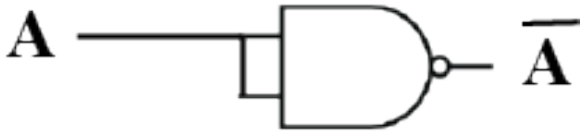
We build its truth table:

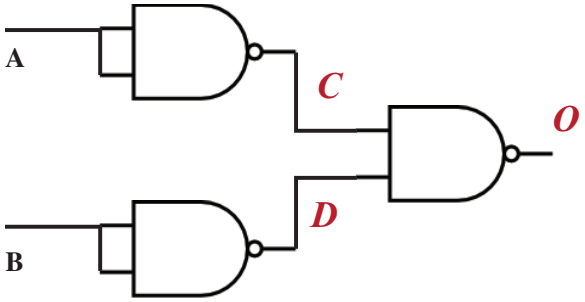
A	B	C	$\bar{B}$	$A\cdot\bar{B}$	$\bar{C}$	$A+B$	$\bar{C}(A+B)$	$A\bar{B}+\bar{C}(A+B)$
1	1	1	0	0	0	1	0	0
1	1	0	0	0	1	1	1	1
1	0	1	1	1	0	1	0	1
1	0	0	1	1	1	1	1	1
0	1	1	0	0	0	1	0	0
0	1	0	0	0	1	1	1	1
0	0	1	1	0	0	0	0	0
0	0	0	1	0	1	0	0	0

Exercise 5

Suppose we wished to have an OR gate for some logic purpose, but did not have any OR gates on hand. Instead, we only had NAND gates in our parts collection. Draw a diagram whereby multiple NAND gates are connected together to form an OR gate.

(*Hint: the NOT gate can be formed using:)*





We build the logic table for this gate:

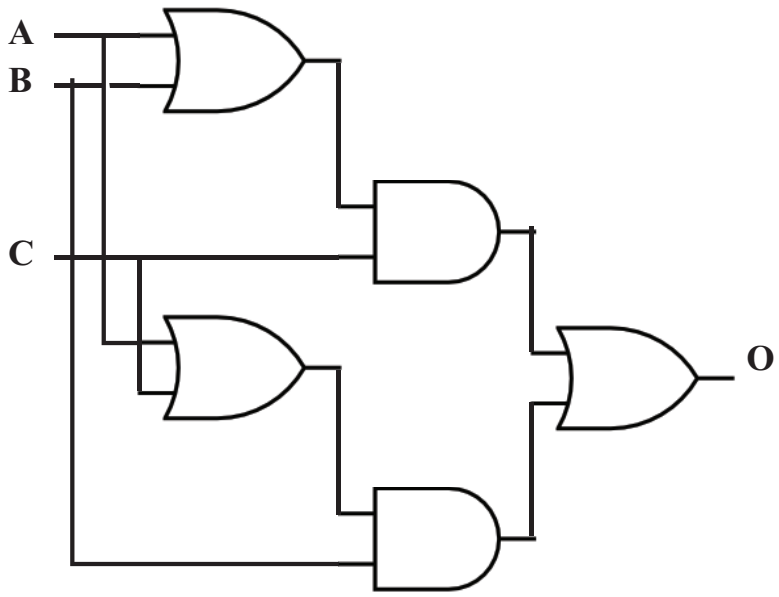
A	B	C	D	O	$A+B$
1	1	0	0	1	1
1	0	0	1	1	1
0	1	1	0	1	1
0	0	1	1	0	0

The output of this gate is fully equivalent to the OR gate.

Exercise 6

*Design a circuit that implements majority voting for three individuals (i.e. the ouput of the circuit is 1 if two at least of the inputs are 1, and 0 otherwise). Build its logic table. (*Hint: consider the Boolean expression $(A+B)\cdot C+(A+C)\cdot B$*).*

One solution is:



To check that this is what we need, we build its logic table:

A	B	C	Expected output	$A+B$	$(A+B)\cdot C$	$A+C$	$(A+C)\cdot B$	$(A+B)\cdot C+(A+C)\cdot B$
1	1	1	1	1	1	1	1	1
1	1	0	1	1	0	1	1	1
1	0	1	1	1	1	1	0	1
1	0	0	0	1	0	1	0	0
0	1	1	1	1	1	1	1	1
0	1	0	0	1	0	0	0	0
0	0	1	0	0	0	1	0	0
0	0	0	0	0	0	0	0	0

$0 = (A+B)\cdot C+(A+C)\cdot B$ is the expected output.