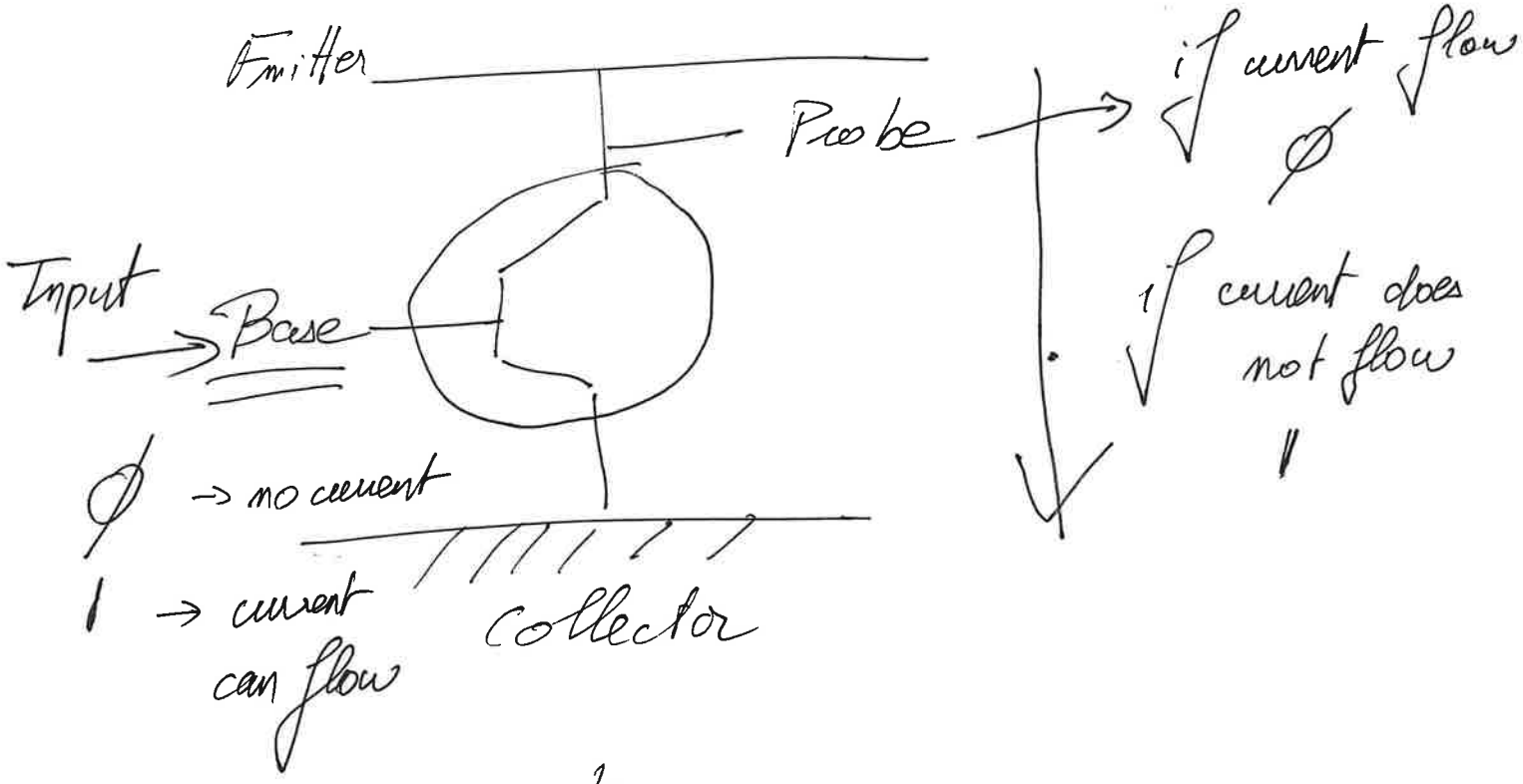
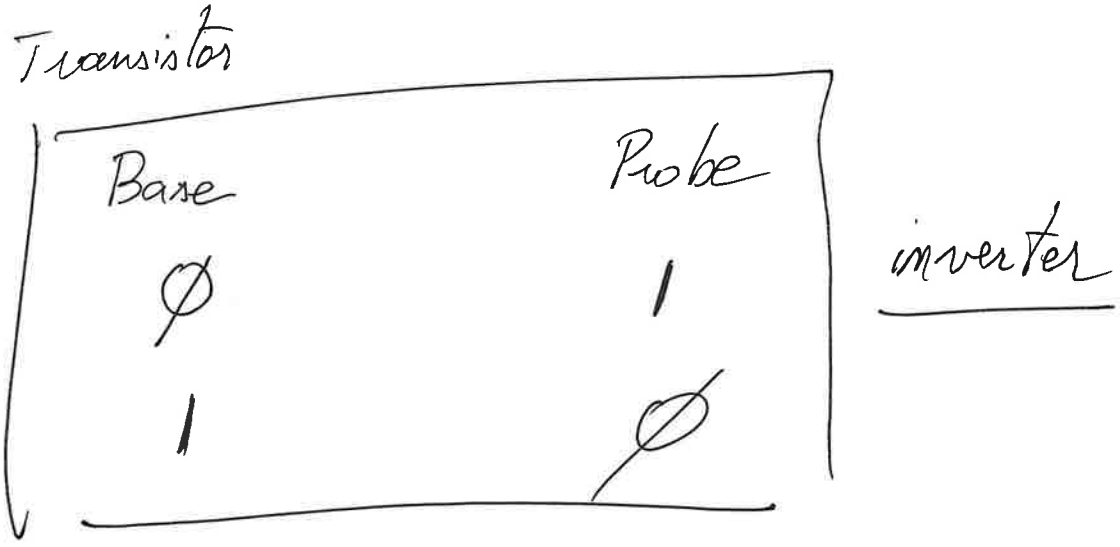
Computing: 1/24/25

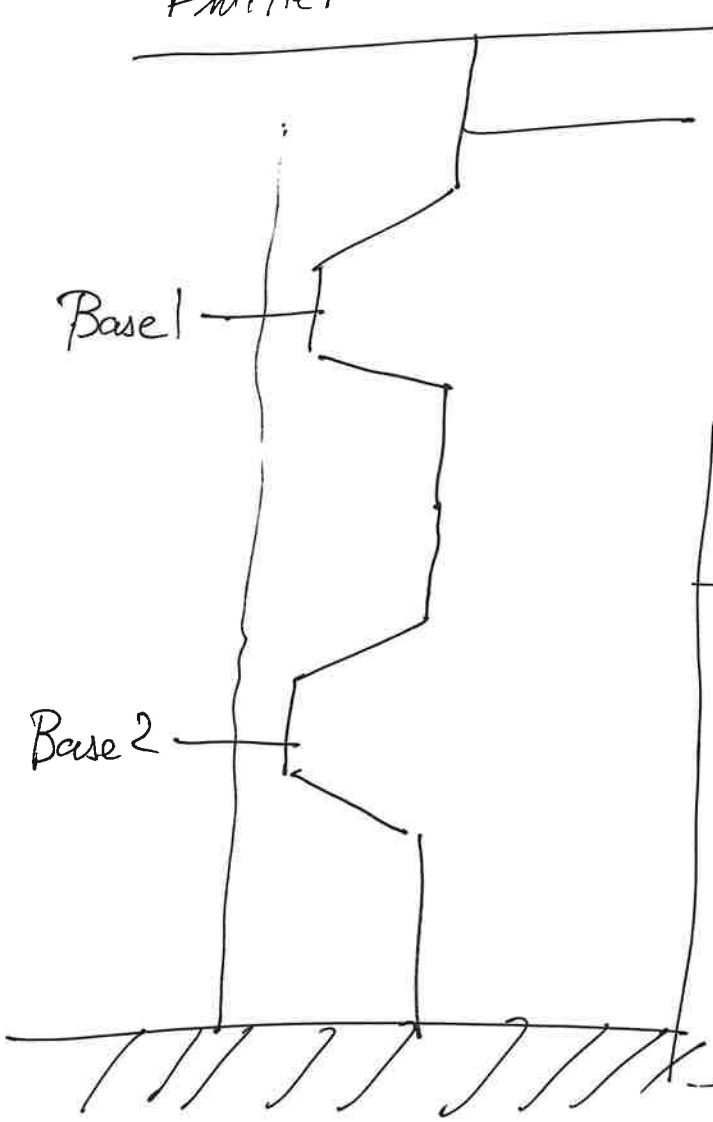
Logic gates

I) Transistor





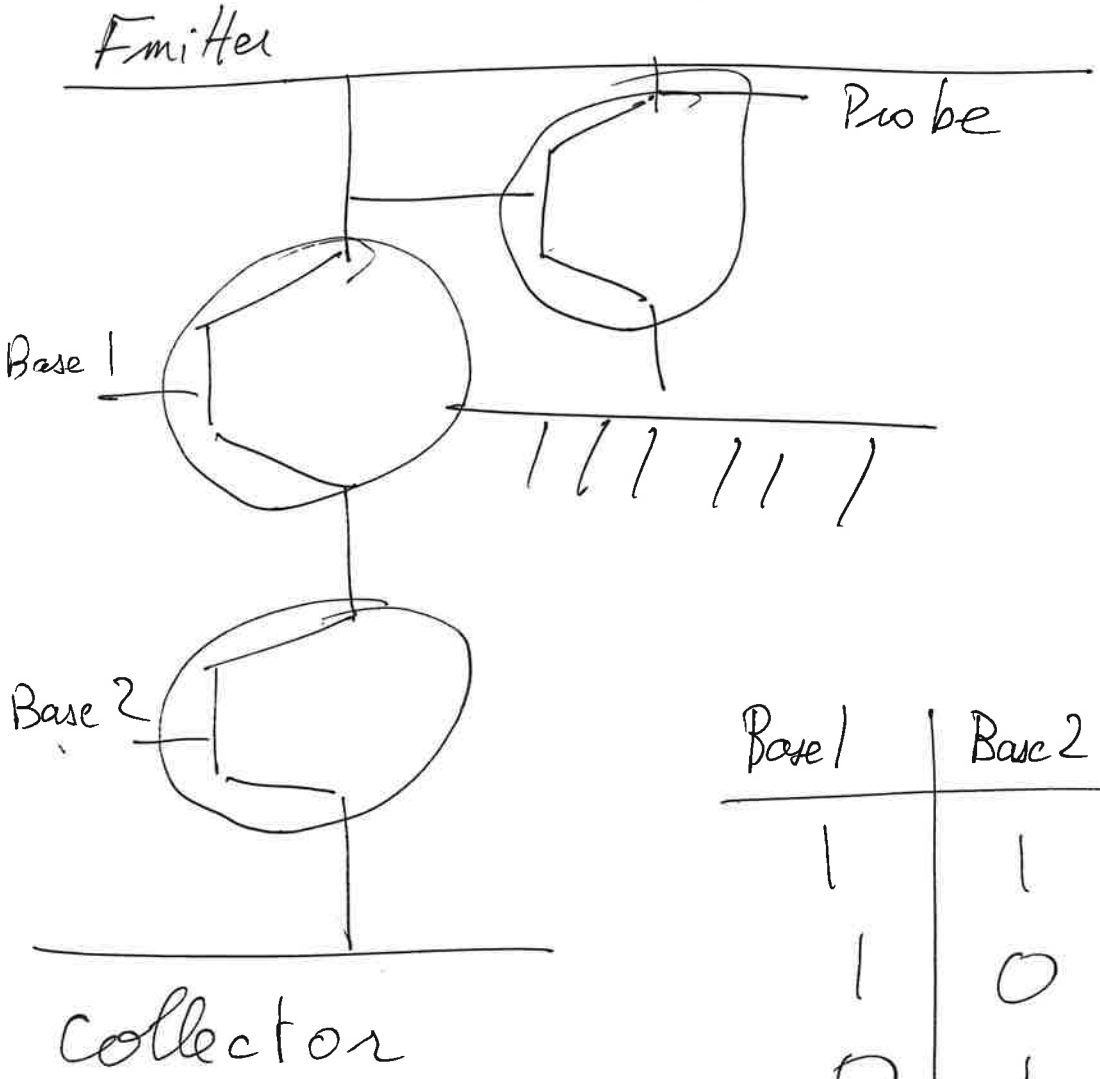
inverter



Base 1	Base 2	Probe
1	1	0
1	0	1
0	1	1
0	0	1

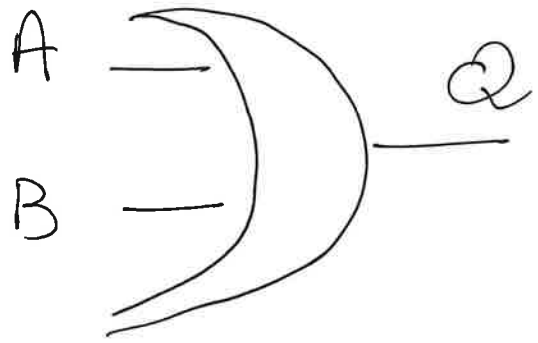
"logic gate"

Base 1	Base 2	Probe
1	1	1
1	0	0
0	1	0
0	0	0



Base 1	Base 2	Probe
1	1	1
1	0	0
0	1	0
0	0	0

3) Or



A	B	Q
1	1	1
1	0	1
0	1	1
0	0	0

Notation : $Q = A + B$

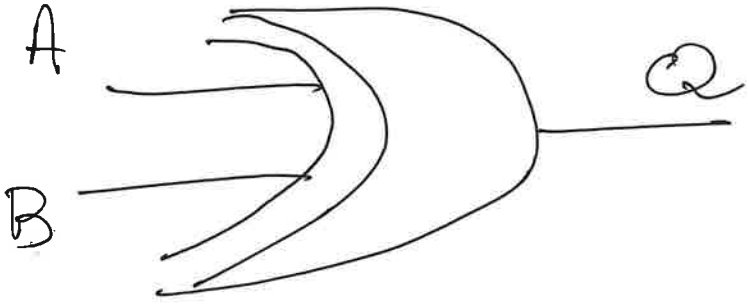
or

$A \vee B$

or

A or B

4) XOR

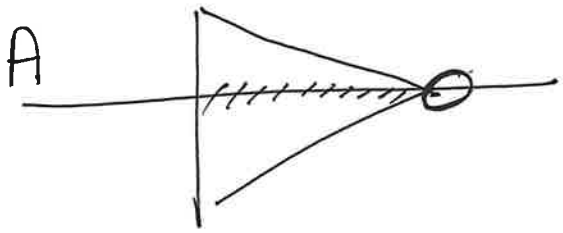


A	B	Q
1	1	0
1	0	1
0	1	1
0	0	0

II Applications

1) Inverter

"Official representation"



A	Q
1	0
0	1

Notation: $Q = \overline{A}$

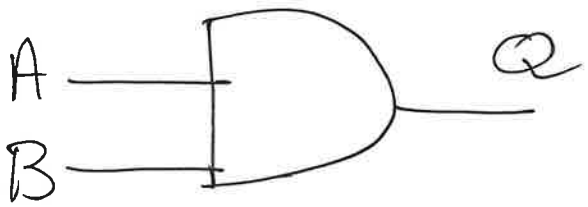
or

$\neg A$

or

not A

2) Multiplication (AND)



A	B	Q
1	1	1
1	0	0
0	1	0
0	0	0

Notation: $Q = A \cdot B$

or $A \wedge B$

or

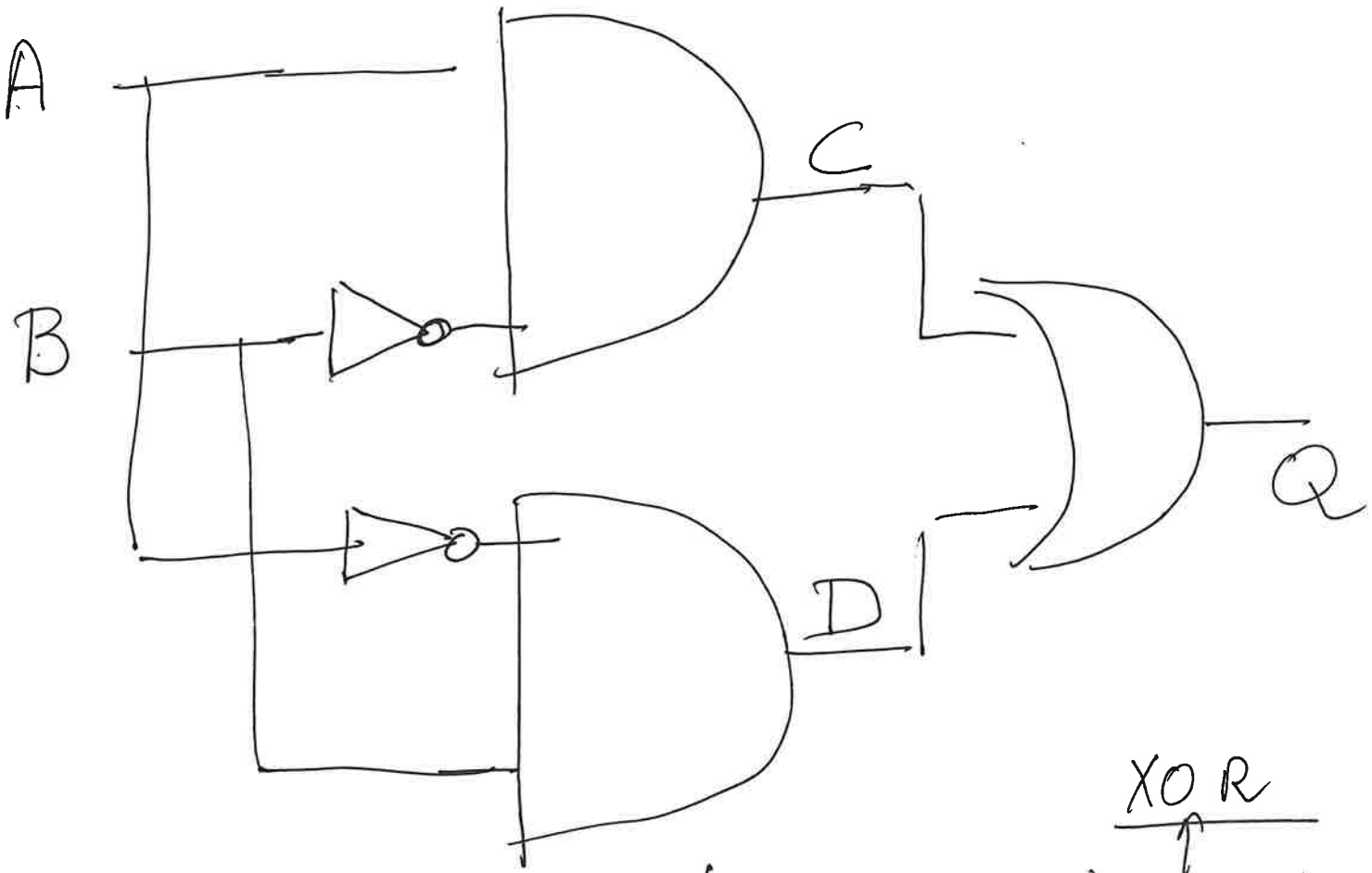
A and B

Building XOR

Consider 2 inputs A and B

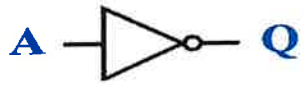
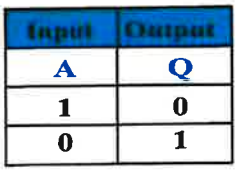
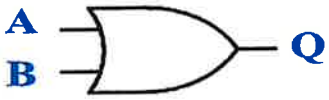
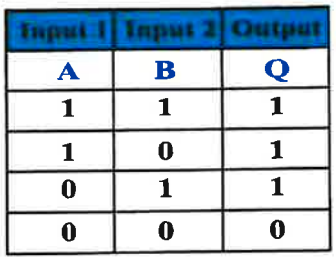
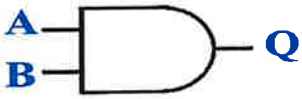
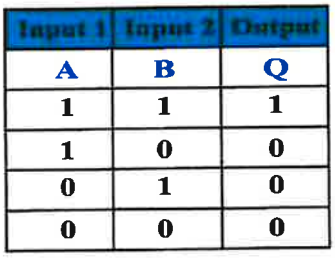
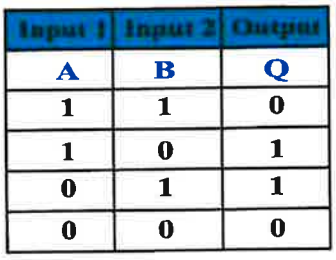
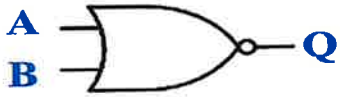
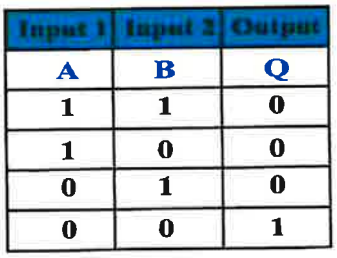
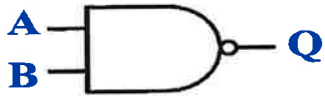
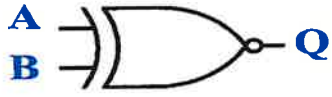
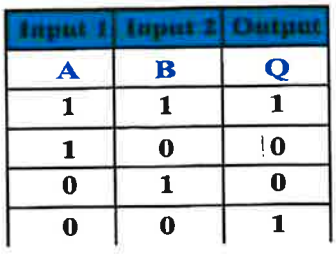
$$Q = A \cdot \overline{B} + \overline{A} \cdot B$$

$$\boxed{A \oplus B = A \cdot \overline{B} + \overline{A} \cdot B}$$



XOR

A	B	$\overline{A}$	$\overline{B}$	C	D	Q
1	1	0	0	0	0	0
1	0	0	1	1	0	1
0	1	1	0	0	1	1
0	0	1	1	0	0	0

NOT		$\overline{A}$ or $\neg A$	
OR		A+B or A∨B	
AND		A•B or A∧B	
XOR		A⊕B	
NOR		$\overline{A+B}$ or $\overline{A \vee B}$	
NAND		$\overline{A \cdot B}$ or $\overline{A \wedge B}$	
XNOR		$\overline{A \oplus B}$	

Input	Output
A	Q
1	0
0	1

Input 1	Input 2	Output
A	B	Q
1	1	1
1	0	1
0	1	1
0	0	0

Input 1	Input 2	Output
A	B	Q
1	1	1
1	0	0
0	1	0
0	0	0

Input 1	Input 2	Output
A	B	Q
1	1	0
1	0	1
0	1	1
0	0	0

Input 1	Input 2	Output
A	B	Q
1	1	0
1	0	0
0	1	0
0	0	1

Input 1	Input 2	Output
A	B	Q
1	1	0
1	0	1
0	1	1
0	0	1

Input 1	Input 2	Output
A	B	Q
1	1	1
1	0	0
0	1	0
0	0	1